AMENDMENT TO THE CLAIMS

In the Claims:

Please **AMEND** claims 1 and 8; and

Please **ADD** new claims 22-26 as follows.

A copy of all pending claims and a status of the claims is provided below.

1. (Currently Amended) A method of fabricating a capacitor, comprising:

forming a bottom electrode;

forming at least one lower surface expansion structure [[to]] on the bottom electrode;

conformally depositing an insulator film to exposed portions of the bottom electrode and at least one lower surface expansion structure; and

forming a top electrode having a planar surface with at least one upper surface expansion structure separated from the at least one lower surface expansion structure by the insulator film,

wherein the at least one lower surface expansion structure and the at least one upper surface expansion structure are vertically arranged.

2. (Original) The method of claim 1, wherein forming a top electrode having a planar surface comprises planarizing a surface of the top electrode by a polishing process.

3. (Original) The method of claim 1, wherein the bottom electrode is capacitively coupled to the top electrode substantially through sides of the at least one lower and upper surface expansion structures.

4. (Original) The method of claim 1, further comprising forming multiple lower surface expansion structures in electrical communication with the bottom electrode by:

forming gaps between the at least one lower surface expansion structures;

exposing sidewalls of the lower surface expansion structures and portions of the bottom electrode;

conformally depositing an insulator film on the portions of the bottom electrode and sidewalls of the multiple lower surface expansion structures; and

forming multiple upper surface expansion structures of the at least one upper surface expansion structure protruding into the gaps and separated from the multiple lower surface expansion structures by the insulator film.

5. (Original) The method of claim 4, wherein the multiple lower surface expansion structures are interleaved with the multiple upper surface expansion structures.

6. (Original) The method of claim 1, wherein the at least one lower surface expansion structure is a first spiral shape and the at least one upper surface expansion structure is a second spiral shape configured to be interleaved with the first spiral shape.

7. (Original) The method of claim 1, further comprising fabricating a second capacitor using the steps of claim 1, and arranging the second capacitor on a top of the capacitor of claim 1.

8. (Currently Amended) The method of claim 1, further comprising:

forming [[a]] another bottom electrode;

forming at least one other lower surface expansion structure to the other bottom electrode;

conformally depositing [[an]] another insulator film to exposed portions of the other bottom electrode and at least one other lower surface expansion structure;

forming a top electrode without at least one upper surface expansion structure separated from the at least one other lower surface expansion structure by the insulator film.

9. (Original) The method of claim 1, wherein the top electrode and the at least one upper surface expansion structures are formed simultaneously.

10. (Original) The method of claim 1, wherein the at least one lower surface expansion structure is formed by:

depositing an interlayer dielectric material on the bottom electrode;

patterning the interlayer dielectric material to form factors;

depositing conductor material into the features such that the conductor material is in content with the bottom electrode;

further patterning the interlayer dielectric material to form gaps between the deposited conductor material.

11. (Original) The method of claim 10, wherein the patterning of the interlayer dielectric layer is one of dual tone resist, sidewall image transfer and masking using self-assembled nanocrystals.

Claims 12-21 (Canceled).

22. (New) The method of claim 1, wherein the at least one upper surface expansion structure is interleaved or interdigitated with the at least one lower surface expansion structure.

23. (New) A method of fabricating a capacitor, comprising:

forming a bottom electrode;

forming a lower surface expansion structure on the bottom electrode, the lower surface expansion structure having a plurality of vertically arranged spaced apart portions;

conformally depositing an insulator film to exposed portions of the bottom electrode and the plurality of vertically arranged spaced apart portions of the lower surface expansion structure; and

forming a top electrode having a planar surface with an upper surface expansion structure having a plurality of vertically arranged spaced apart portions,

wherein the upper surface expansion structure is separated from the lower surface expansion structure by the insulator film.

24. (New) The method of claim 23, wherein the plurality of vertically arranged spaced apart portions of the upper surface expansion structure is interleaved or interdigitated with the plurality of vertically arranged spaced apart portions of the lower surface expansion structure.

25. (New) A method of fabricating a capacitor, comprising:

forming a bottom electrode;

forming a first plurality of vertically arranged spaced apart expansion structures on the bottom electrode;

conformally depositing an insulator film to exposed portions of the bottom electrode and the first plurality of vertically arranged spaced apart expansion structures; and

forming a second plurality of vertically arranged spaced apart expansion structures in spaces between the first vertically arranged spaced apart expansion structures;

forming a top electrode having a planar surface on the second plurality of vertically arranged spaced apart expansion structures.

26. (New) The method of claim 25, wherein the first plurality of vertically arranged spaced apart expansion structures is interleaved or interdigitated with the second plurality of vertically arranged spaced apart expansion structures.